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Scaling of Coplanar Homojunction Amorphous In–Ga–Zn–O Thin-Film Transistors

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Channel length (L) and width (W) scaling of amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs) have been investigated by coplanar homojunction a-IGZO TFTs. The fabricated TFTs have a mobility around 12 $cm^2 V^{-1} s^{-1}$, sub-threshold slope (S) of ~110 mV/decade, threshold voltage around 0.3 V and off-current below 10^{-13} A. The TFTs with $L > 5$ µm have the reduced transconducance (g_m) at lower V_{GS}, however, the short $L < 5$ µm TFTs have the g_m reduction at higher V_{GS}. Even though the TFTs with smaller channel length ($L \leq 5$ µm) show proper switching characteristics, threshold voltage lowering and sub-threshold slope degradation are clearly observed.
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1. Introduction

High resolution (beyond 1920 × 1080), high pixel density (≥300 pixels per inch, PPI), large panel size (≥80-in.) and a fast frame rate (≥240 Hz) have become key features of future technology in the area of active matrix flat panel displays (AM-FPD). The essential requisite for achieving these features is a high field-effect mobility μ of thin-film transistors (TFTs). This is because a higher μ induces a higher drain current, so enabling the TFTs to switch faster and/or occupy a smaller pixel area. It is estimated that the ultrahigh-definition (7680 × 4320) television (UHD TV or 8K TV) with 120 Hz of refresh rate requires μ over 3 $cm^2 V^{-1} s^{-1}$.[1)] The hydrogenated amorphous silicon (a-Si:H) TFTs are not adequate for such a high resolution application because μ of a-Si:H TFTs has the range of 0.5–1 $cm^2 V^{-1} s^{-1}$.[2,3)] In this regard, amorphous indium–gallium–zinc–oxide (a-IGZO) TFTs have received considerable attention as a possible replacement for a-Si:H TFTs.[4–7)] Thanks to previous intensive research studies on a-IGZO TFTs, it has been proved that a-IGZO TFTs with μ over 5 $cm^2 V^{-1} s^{-1}$ can be easily fabricated.[8–10)]

Besides the mobility requirement, TFT miniaturization is another important factor for high pixel density applications. Since an allowed pixel size decreases as the PPI increases — the pixel size for 500 PPI is only 50.8 × 16.9 μm^2, for instance — the TFT needs to be scaled down along with the pixel size to be fitted inside of the pixel area. This situation is even worse in active-matrix organic light emitting display (AM-OLED) because at least two TFTs must be squeezed in each pixel area.[11)] Furthermore, it is known that the miniaturization of TFTs improves the display performance by reducing the parasitic capacitance. The high mobility and miniaturization requirements are also critical for the high resolution active matrix flat panel imager (AM-FPI), especially for the application of digital radiology.[12,13)] Even though a-IGZO TFTs with an L smaller than 5 µm were previously reported by other groups,[14)] a systematic study of the scaling of a-IGZO TFTs has been lacking. Therefore, it is worthwhile to investigate the scaling characteristics of a-IGZO TFTs.

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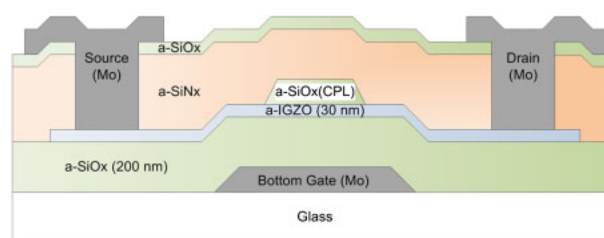
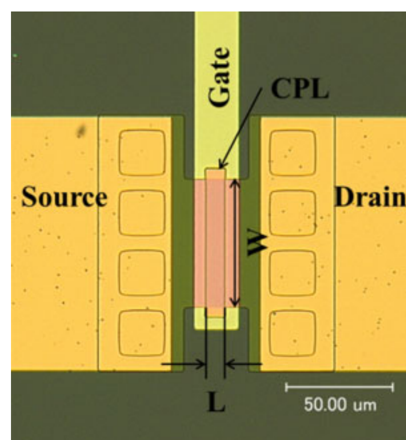


(a)



(b)

Fig. 1. (Color online) (a) Schematic cross-sectional structure of the coplanar homojunction a-IGZO TFT, (b) macroscopic top view of the fabricated TFT. CPL defines channel length (L) and width (W) of the TFT.

In this paper, we present an in-depth study of the scaling dependency of coplanar homojunction a-IGZO TFTs. The coplanar homojunction a-IGZO TFTs investigated in this paper utilize a hydrogen doped a-IGZO source/drain (S/D) region, n^+ a-IGZO, to achieve a low resistance S/D contacts. It was previously reported that this structure has the advantages of small S/D contact resistance and the capability of achieving a small L.[15)] Therefore, the scaling characteristics for this type of a-IGZO TFT is worthwhile to be investigated.

2. Methods

A cross-sectional schematic of the fabricated TFT is shown in Fig. 1(a). The TFTs were fabricated on a Corning 1737 glass

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substrate. The Mo layer (100 nm) was sputtered as the gate electrode. Amorphous silicon oxide (a-SiO_x) layer (200 nm) was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 340 °C as a gate insulator. The a-IGZO layer (30 nm) was deposited by DC sputtering and the a-SiO_x layer (100 nm) was deposited by RF magnetron sputtering as a channel protection layer (CPL). The CPL defines the TFT's length (L) and width (W). Figure 1(b) clearly shows the top view of the CPL taken under an optical microscope, showing the well-defined channel W and L of 60 and 10 μm, respectively. A 300-nm-thick hydrogenated amorphous silicon nitride (a-SiN_x:H) and a 50-nm-thick a-SiO_x are deposited sequentially in this order by PECVD at 250 °C as a protection layer on top of the CPL and a-IGZO (not covered with CPL) regions. During the deposition process of a-SiN_x:H layer, the exposed areas of the a-IGZO layer were converted into low resistance S/D through doping of a-IGZO region by hydrogen. Next, the S/D contacts were formed in a top passivation layer by dry etching, followed by the sputtering of 100-nm-thick Mo S/D electrodes defined by wet etching. In this structure, gate metal and S/D contact do not overlap; although there is some overlap between the gate and the hydrogen doped S/D contact regions.

All measurements were carried out in a dark box using Agilent 4156C semiconductor parameter analyzer. The ideal metal–oxide–semiconductor field-effect transistors (MOSFET) drain current against gate-to-source voltage (I_D–V_{GS}) equation is used to extract the device parameters in the linear operation region:[16)]

$$I_D = \mu C_G \frac{W}{L}(V_{GS} - V_{TH})V_{DS}, \qquad (1)$$

where C_G is the capacitance per unit area of the gate insulator. The best linear fit of I_D–V_{GS} curves between 10 and 90% of maximum I_D is used for μ and V_{TH} extraction. The V_{TH} is the threshold voltage, and V_{DS} and V_{GS} are drain-to-source and gate-to-source voltage, respectively. For the saturation region ($V_{DS} = 15$ V), the following $I_D^{1/2}$–V_{GS} equation is used:[16)]

$$I_D^{1/2} = \sqrt{\frac{1}{2}\mu C_G \frac{W}{L}}(V_{GS} - V_{TH}). \qquad (2)$$

The sub-threshold swing (S) is defined as $S = (\partial \log I_D/\partial V_{GS})^{-1}$ at around a maximum $(\partial \log I_D/\partial V_{GS})^{-1}$ point. The leakage current, I_{OFF}, is defined as I_D when $V_{GS} = -10$ V. The above equations are programmed in MATLAB software from MathWorks and used for extracting all TFTs' parameters. The TFTs over uniformly distributed six dies on the same substrate are selected as samples. The average and standard deviation values of the extracted parameters are used for the discussion later presented here.

3. Channel Length Scaling

To study the channel length dependency of TFTs, the I_D–V_{GS} and $I_D^{1/2}$–V_{GS} curves with various Ls (from 3–120 μm) are shown in Fig. 2. The W is fixed at 60 μm. From Fig. 2, we conclude that all TFTs demonstrate normal TFT operation and that the TFT's I_D increases with decreasing channel length. This is in agreement with the ideal equations [Eqs. (1) and (2)].

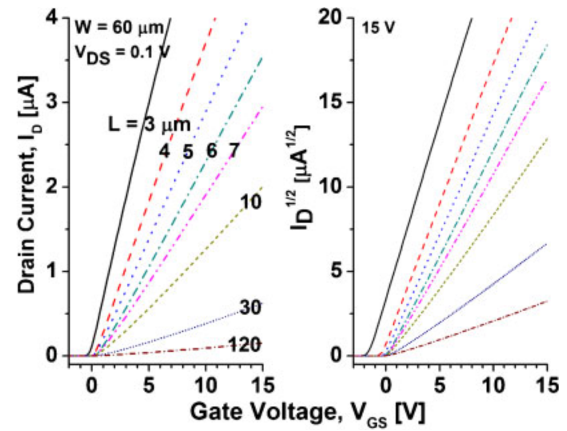

Fig. 2. (Color online) I_D–V_{GS} and $I_D^{1/2}$–V_{GS} curves with various channel length. The channel width is fixed at 60 μm.

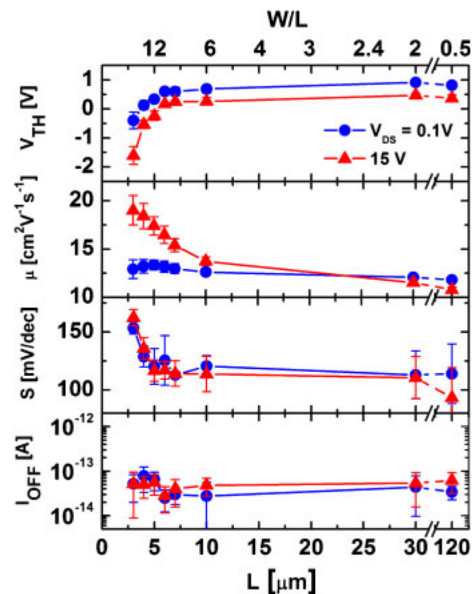

Fig. 3. (Color online) Channel length dependency of V_{TH}, μ, S, and I_{OFF}.

Beside current–voltage curves, various TFT parameters should be investigated to understand the channel length dependency. The key parameters, such as V_{TH}, μ, S, and I_{OFF}, of TFTs are summarized as a function of L in Fig. 3. With a shorter L, the V_{TH} decreases and S increases (i.e., becomes less steep). These changes become more severe when the TFT's L is smaller than 5 μm. Furthermore, it should be noted that small L TFTs ($L < 5$ μm) work as a depletion mode ($V_{TH} < 0$ V) device while large L TFTs ($L \geq 5$ μm) work as an enhancement mode ($V_{TH} > 0$ V) device in the saturation region. The similar changes in V_{TH} and S have been easily observed in short channel MOSFETs which are not scaled properly. The off-current of a-IGZO TFTs does not change with a smaller channel length, while the off-current increases linearly in a-Si TFTs.[17)] This is attributed to the low hole-density in a-IGZO material.

We describe the mobility variations associated with different channel lengths. The mobility of a-IGZO TFTs is almost constant in the linear region. However, the saturation region mobility increases in short channel length TFTs. The

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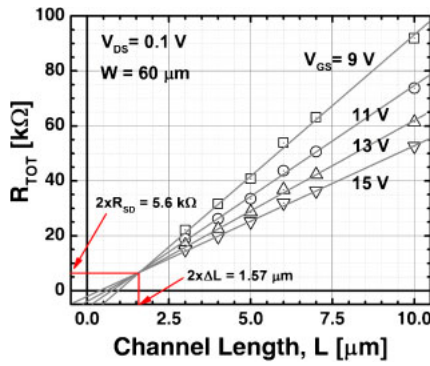

Fig. 4. (Color online) Illustration of the transmission line method. Symbol: experimental data, solid line: linear fit to the TLM model.

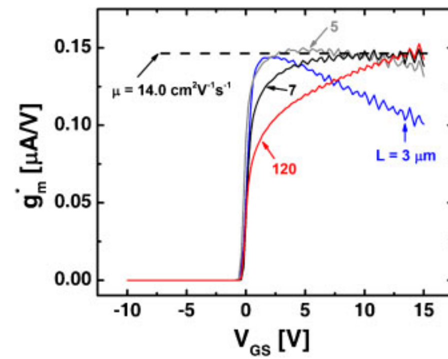

Fig. 5. (Color online) The dimension normalized transconductance are plotted for $L = 3$, 5, 7, and 120 μm ($V_{DS} = 0.1$ V).

physical reason for the increase of mobility in the saturation region is that the high V_{DS} bias increases the channel length modulation ΔL, and decreases the effective channel length ($L_{eff} = L - \Delta L$). Moreover, the effect of ΔL becomes significant for small L TFTs. This is equivalent to saying that the effective channel length is smaller than the physical channel length, the calculated μ shows a higher value than what it actually should have. This difference gets larger as L decreases. At this point, the mobility dependency of a-IGZO TFTs is worthwhile to compare with that of a-Si:H TFTs. Mobility degradation has been observed for short channel a-Si:H TFTs. This effect is due to the increased magnitude of the S/D resistance (R_{SD}) for short channel a-Si TFTs.[18,19] However, in coplanar homojunction a-IGZO TFTs, such degradation due to high S/D resistance is not severe.

To confirm the low R_{SD} in coplanar homojunction a-IGZO TFTs, R_{SD} and channel length modulation (ΔL) are extracted using the transmission line method (TLM) when $V_{GS} - V_{TH} \gg V_{DS}$ (also known as channel-resistance or current–voltage method)[20] (Fig. 4):

$$R_{TOT} = \frac{V_{DS}}{I_D} = 2 \times R_{SD} + \frac{L - 2 \times \Delta L}{\mu C_G W (V_{GS} - V_{TH})}. \quad (3)$$

In this measurement, a V_{DS} of 0.1 V is used to satisfy the requirement of $V_{GS} - V_{TH} \gg V_{DS}$. For our coplanar homojunction a-IGZO TFTs, the cross-point is located in the first (I) quadrant where ΔL is positive. This is equivalent to saying that "$L_{eff} < L$", which implies that the S/D hydrogen doping region is horizontally diffused into the channel region and/or CPL patterns are shrunk from its drawn length during lithography or etching process. Similar observation was also made for self-aligned top gate TFTs, which have the shortened effective channel length.[21] The evaluated $2 \cdot R_{SD}$ and $2 \cdot \Delta L$ are 5.6 kΩ and 1.57 μm, respectively. These values are consistent with previously reported values.[15] Hence, we confirm that the a-IGZO region, not covered by CPL, makes good ohmic contacts with Mo and the width-normalized contact resistance ($R_{SD} \cdot W$) is 16.8 Ω·cm for $W = 60$ μm. It should be noticed that in the proposed TFT structure, the S/D contact area is composed of (i) overlap between gate metal and heavily doped a-IGZO region (n^+ a-IGZO), (ii) n^+ a-IGZO extension region to S/D metal, and (iii) interface between S/D metal and n^+ a-IGZO film.

To obtain further insights into short channel TFTs, we also investigated the changes in the dimension-normalized transconductance [$g_m^* = \partial(I_D \times L/W)/\partial V_{GS}$, $V_{DS} = 0.1$ V]. The transconductance is plotted as a function of V_{GS} in Fig. 5. For TFTs with $L = 3$ μm, the g_m^* reaches a maximum at the point of inflection of the I_D–V_{GS} curve, and then decreases. This decrease can be explained by two factors: degradation of μ as a function of an increasing transverse electric field across the gate dielectric and/or a voltage drop ($V = I_D R_{SD}$) associated with the large current. Since this phenomenon is not observed in large L TFTs, we conclude that this behavior is affected by the voltage drop. For TFTs with $L = 5$ μm, the g_m^* is rather constant under TFT's ON state. In contrast, in TFTs with $L = 120$ μm, the g_m^* keeps increasing without having a maximum point, which has been commonly observed by many labs for a-IGZO TFTs. This is speculated that TFTs with large L suffer from a large channel resistance (R_{ch}) at smaller V_{GS}, which is due to decreased-current associated with charge trapping/scattering by oxygen vacancies. In addition, we find that the maximum transition points of g_m^* are all similar (near 0 V). Therefore, the V_{TH} reduction in Fig. 3 is originated from the limitation of the linear extraction method of V_{TH}. In short, the IR drop and charge trapping/scattering are the reasons of g_m^* degradation for short and long L TFTs, respectively. This implies that there is the optimum channel length, which has a minimized influence from those two effects, and the TFT will have the highest μ value at this point. From Fig. 3, we find that $L = 5$ μm is the optimal point in the fabricated TFT structure.

When higher drain voltage ($V_{DS} = 15$ V) is applied on TFTs, the V_{TH} reduction is more severe than at $V_{DS} = 0.1$ V. Furthermore, the degradation of S is clearly observed for TFTs with short L. The V_{TH} reduction at higher V_{DS} and S degradation cannot be explained by the g_m^* discussed in the above paragraph. The similar observations of V_{TH} and S changes, however, have been made in short channel MOSFETs which are not scaled properly. From the scaling theory of transistors,[22] it is known that the thickness of gate dielectric must decrease (equivalently increasing gate capacitance per unit area, C_G) with the same ratio of the channel length scaling, so maintaining the gate controllability even in shorten channel length. In addition, recent studies show that double-gate TFTs can have increased effective C_G without decreasing the dielectric thickness.[23] The effect of

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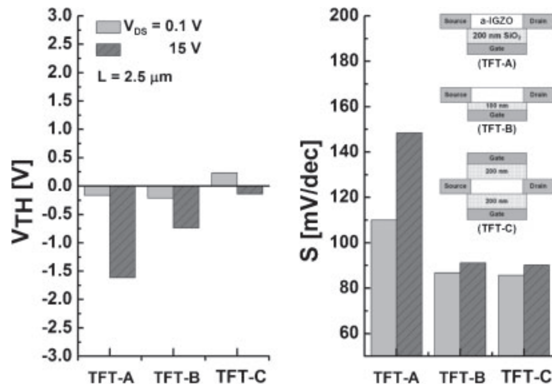

Fig. 6. The comparison of V_{TH} and S for three different TFT structure: (TFT-A) bottom gate TFT with 200-nm-thick SiO_2, (TFT-B) bottom gate TFT with 100-nm-thick SiO_2, and (TFT-C) double gate TFT with 200-nm-thick SiO_2.

different gate capacitance was studied by the device simulation using an ATLAS two-dimensional device simulator from Silvaco Inc. The previously reported simulation parameters for the density of states are adopted for this study.[24] Figure 6 shows the V_{TH} and S dependency of TFT having different gate capacitance: TFT-A and -B correspond to TFTs with 200 and 100 nm thickness of the gate dielectric (SiO_2), respectively, and TFT-C represents the double gate TFT. The thickness for both the top and bottom gate dielectric is 200 nm for the double gate TFT. The channel length of TFTs is fixed at 2.5 μm. From the simulated I–V curves, the V_{TH} and S are extracted in the same manner as described in Sect. 2. As can be seen in Fig. 6, V_{TH} reduction and S degradation is observed for TFT-A. However, the V_{TH} reduction is improved for the structures of TFT-B and -C. We expect that the increase of C_G prevent the barrier lowering, which is induced by the drain voltage. The changes in S can be explained by the increased portion of source-to-drain electric field. From the two dimensional Poisson's equation,

$$\frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} = \frac{\rho}{\varepsilon}, \quad (4)$$

where E_x and E_y are the electric field in channel region in vertical (gate-to-channel) and horizontal (source-to-drain) directions, respectively. ρ is the charge density per unit area at a given coordinate, x and y, and ε is the permittivity at the given coordinate. For the same C_G, the first term $(\partial E_x/\partial x)$ of Eq. (4) is same for TFTs with different L, and its quantity is small for the sub-threshold regime. The second term $(\partial E_y/\partial y)$ is negligible for long channel TFTs; in other words, ρ is small and mostly controlled by the gate field. However, in case of TFTs with short L, the second term becomes significant because E_y is increasing as L decreases. The increased quantity of the second term contributes a higher ρ, which is related to less steep S. However, the increased C_G (or increased gate controllability) makes the first term dominant again and minimized the second term, which has L dependency. This is consistent with the simulation results. Therefore, we conclude that specific TFT structure, such as double gate structure, or the thickness control of gate dielectric layer must be introduced for the short channel TFTs.

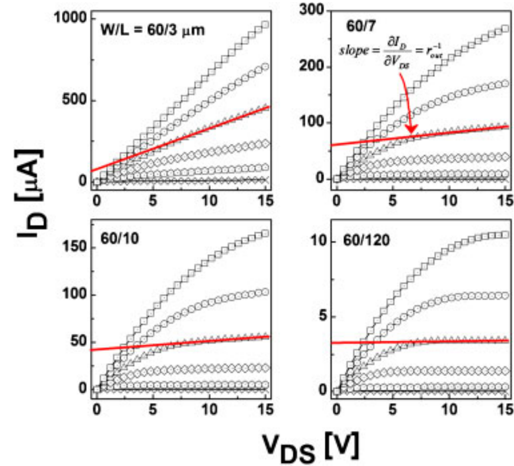

Fig. 7. (Color online) I_D–V_{GS} (dots) and output resistance (solid line) are plotted for $L = 3$, 7, 10, and 120 μm.

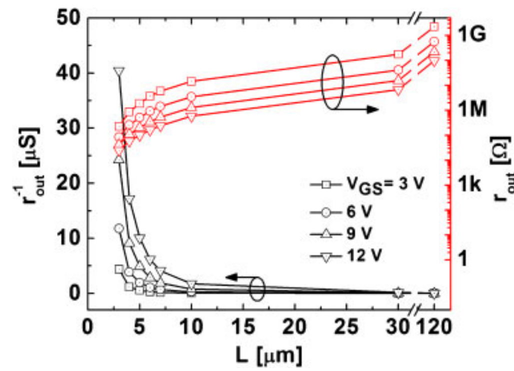

Fig. 8. (Color online) Channel length dependency of the output resistance.

Lastly, the output characteristics of TFTs are shown in Fig. 7. It is observed that reducing the channel length below 5 μm results in an apparent deviation of the output characteristics from their solid saturation. In other words, the output resistance r_{out} rapidly decreases for $L \leq 5$ μm. The r_{out} is defined by the following equation in the device saturation region:

$$r_{out} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \text{(in saturation).} \quad (5)$$

The channel length dependency of r_{out} is summarized in Fig. 8 for a different V_{GS}. The r_{out} is an important parameter for designing amplifiers. The common source amplifier or common drain amplifier can be used as a gate driver or amplifier in AM-FPDs or AM-FPIs.[11,13,25] Figure 9 shows the circuit schematics of common source and common drain N-TFT amplifiers. Since a-IGZO TFTs are unipolar in nature, an N-type circuitry is suitable rather than a complementary type circuitry. The voltage gain (A_V) of the common source and common drain amplifier are described as

$$A_V = -g_m(r_{out} \mathbin{//} R_D) \text{ and } A_V = \frac{g_m}{g_m + 1/(r_{out} \mathbin{//} R_S)}, \quad (6)$$

respectively. Therefore, a smaller r_{out} results in a smaller gain. In the worst case, $r_{out} \ll R_D$, R_S, the gain of the

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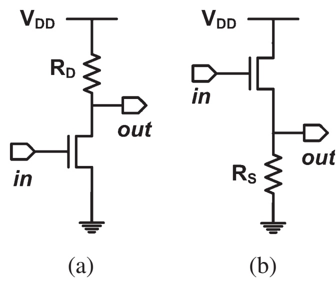

Fig. 9. Circuit schematics for n-TFT (a) common source amplifier and (b) common drain amplifier.

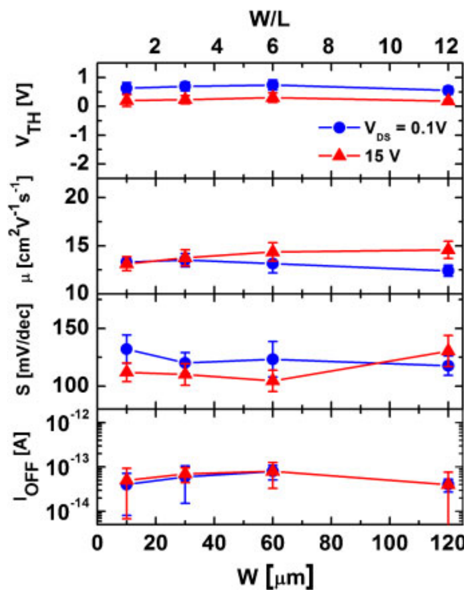

Fig. 10. (Color online) Channel length dependency of V_{TH}, μ, S, and I_{OFF}.

amplifier is mostly controlled by parasitic resistance (r_{out}) rather than design resistance (R_D or R_S).

4. Channel Width Scaling

Similar analysis is done for various Ws (from $10 \leq W \leq 120\,\mu m$). L is fixed at $10\,\mu m$. The device parameters of a-IGZO TFTs are shown in Fig. 10. Although the channel width is varied from 1× to 12× channel width, we do not observe noticeable changes in the TFT parameters. Therefore, the channel width is not a serious design consideration because the channel width, which is larger than the channel length, is usually used in the circuit design.

5. Summary

In summary, we have studied the scaling characteristics of coplanar homojunction a-IGZO TFTs with 200-nm-thick PECVD a-SiO$_x$. For long channel TFTs, the current reduced at low V_{GS}. In contrast, the current reduction occurs at high V_{GS} for short channel TFTs. It would seem that the charge trapping/scattering and IR drop are at the origin of TFT channel length dependency. The $5\,\mu m$ is the optimal L for TFT structure studied in this work without suffering these two degradations. However, this optimal channel length could be different for different TFT structures, such as different dielectric material/thickness and metal contacts. In the case of TFTs with $L \leq 5\,\mu m$, r_{out} and S degrade rapidly and negative V_{TH} is observed, and we conclude that is due to the weaken channel controllability of the gate for short channel TFTs. To achieve small L TFTs without any performance degradation, the gate dielectric should be scaled properly or a double-gate device structure must be used. We did not observe any noticeable W dependency for coplanar a-IGZO TFTs.

Acknowledgement

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